

APPARATUS AND METHOD FOR TRACE
STREAM IDENTIFICATION OF A
PROCESSOR DEBUG HALT SIGNAL

Abstract of the Invention

1 When a DEBUG HALT signal is generated in a target processor
2 during a test procedure, a debug halt sync marker is
3 generated in a program counter trace stream. The debug
4 halt sync marker includes a plurality of packets, the
5 packets identifying that the sync marker is the result of a
6 DEBUG HALT signal. The packets also identify the program
7 counter address at the time of the generation of the DEBUG
8 HALT signal and relate the debug halt sync marker to a
9 timing trace stream.

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